Amendments to the Specification:

Please replace the paragraph, beginning at page 2, line 5, with the following rewritten paragraph:

B1

The error flags are written into and read from the receiver FIFO circuit together with received data. Accordingly, the ~~LSR 7 bits~~ LSR7 bit changes in state when the received data is written into and read from the receiver FIFO circuit.

Please replace the paragraph, beginning at page 4, line 13, with the following rewritten paragraph:

B2

~~The 1st invention~~ One aspect of the present invention is an asynchronous FIFO circuit comprising:

Please replace the paragraph, beginning at page 5, line 10, with the following rewritten paragraph:

B3

~~The 2nd invention~~ Another aspect of the present invention is an asynchronous FIFO circuit comprising:

Please replace the paragraph, beginning at page 7, line 3, with the following rewritten paragraph:

B4

~~The 3rd invention~~ Still another aspect of the present invention is the asynchronous FIFO circuit ~~according to 1st or 2nd inventions~~, wherein said error write counter and said error read counter are formed of a gray code counter.

Please replace the paragraph, beginning at page 7, line 7, with the following rewritten paragraph:

B5

~~The 4th invention~~ Yet still another aspect of the present invention is an asynchronous FIFO data reading and writing method comprising:

Please replace the paragraph, beginning at page 8, line 1, with the following rewritten paragraph:

B6

~~The 5th invention~~ Still yet another aspect of the present invention is an asynchronous FIFO data reading and writing method comprising:

Please replace the paragraph, beginning at page 9, line 20, with the following rewritten paragraph:

B7

~~The 6th invention~~ A further aspect of the present invention is the asynchronous FIFO data reading and writing method ~~according to 4th or 5th inventions~~, wherein said error write step and said error read step are formed of a gray code count step.

Please replace the paragraph, beginning at page 15, line 7, with the following rewritten paragraph:

B8

Reference numeral 61 denotes an error write counter that is formed of an N-bit counter. When a word having at least one of the error flags set to 1 is written into the memory 23, the error write counter 61 counts up by 1 upon a write signal WR as a clock. When the error write counter 61 counts up from 2^N-1, the error write counter 61 is reset to 0, or wraps around to 0. Therefore, the value of error write counter 61 is equal to a remainder when an accumulated number of times that a word having at least one of the error flag set to 1 is stored into the memory 23 is divided by 2^N. N is a positive integer such that $N=\log_2$ (number of locations in the memory)~~such that the number of words in the memory 23 is divided by 2^N~~. In the present embodiment, N=3.